Design of a Net-Zero Charge Neural Stimulator with Feedback Control

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***Abstract*—This paper presents a high efficiency, net-zero charge neural stimulator. A new stimulation strategy is proposed to reduce the charge error that originates from the irreversible charge diffusion, which is a common issue in traditional current matching stimulator designs. In addition, an arbitrary channel configuration of the working and counter electrodes is achieved. Two methodologies are applied to the proposed design to increase the stimulation efficiency: i) feedback control of an adaptive driving voltage, which enables a constant low operating voltage for the entire active circuits; ii) charge recycling, which "recycles" the accumulated charges on the blocking capacitor. An improved current mode DAC and a digital feed-forward error compensation comparator are integrated in the output stage to suppress the process variation, and minimize the charge error in continuous stimulation pulse trains. Performance characterization and in-vivo experimental result of a prototype chip fabricated in standard 180nm CMOS technology are presented. An efficiency improvement of 51% is measured in the experiment.**

I. Introduction

Chronic neural stimulation shows a promising treatment for patients suffering from neurological injury or disease, and also can provide continuous sensory feedback from the prosthesis. However, high duty-cycle electrical stimulation's safety issues and high system power consumption are the bottlenecks in developing fully implantable neural stimulators. During a electrical stimulus, both polarizable and non-polarizable mechanisms of charge transfer occur at the interface between the electrode and the physiological medium [1]. Since the irreversible non-polarizable charge transfer may cause damaging chemical species and dissolve electrodes, it is critical to avoid the onset of these reactions. A reversal phase is usually used to reverse the electrochemical processes right after the stimulation phase. Voltage-controlled [2], current-controlled [3–5], and charges-controlled [6] stimulation methods have been reported in literature. The voltage-controlled stimulation method features the highest efficiency, but it is difficult to control the total amount of the injected charges [7]. The charges-controlled stimulation limits the total amount of the inject charges by discharging a series of capacitors, but the capacitors cost large area and the discharging time cannot be precisely controlled. The current-controlled stimulation has a high controllability of the charge injection, thus is the most widely used method. However, the power efficiencies in conventional designs are usually lower than the other methods.

Current-controlled stimulation can be implemented in dual supply voltages [8] or single supply voltage [9]. In practice, current source and sink which drive the stimulating and reversal currents are typically mismatched by about 1%- 2% due to the non-idealises in the fabrication [3]. Many low charge error stimulation methods have been reported in literature [3–5, 10, 11], focusing on the matching of the stimulating and reversal currents to achieve the net zero charges. However, the unrecoverable charge injection during stimulating pulse has been ignored. This work proposes a method to realize the net-zero charge by employing a feedback control. An arbitrary channel configuration of the working and counter electrodes is achieved without a pre- or on the fly calibration. Given the low efficiency of the conventional current-controlled stimulation, two methodologies are proposed in this work to increase the stimulation efficiency: i) a feedback control of the adaptive driving voltage, which enables a constant low supply voltage for all active circuits, and ii) a charge recycling of the accumulated charges from the stimulating phase for use in the reversal phase. A current mode DAC with a threshold variation cancellation technique is integrated in the output stage to improve the linearity and suppress the variation across the driving site array. A digital feed-forward error compensation mechanism is used to calibrate the zero-crossing detection comparator in a continuous stimulation pulse train.

The remaining sections of the paper are organized as follows. Section II describes the proposed stimulation strategy. Section III presents the architecture design and the circuit implementation. Experimental results are presented in Section IV, while Section V concludes the whole paper.

II. Design of the Net-Zero Charge Stimulator

In the implementation of a biphasic current stimulation, in order to achieve the net-zero charge, a reversal phase is applied after the stimulating phase, and an interphase delay is inserted between these two phases to suppress the reverse of the desired physiological effect. However, even well calibrated stimulator output stages will still leave residue charges due to the unrecoverable charge diffusion in the stimulating phase, which requires an additional discharge phase, as shown in Fig. 1(a). In this work, the reversal phase terminates when a net-zero charge point is detected, as shown in Fig. 1(b). An arbitrary channel configuration of the working electrodes (WE) and the counter electrodes (CE) is feasible in this strategy since no calibration is required for the current sources and sinks. C_n^2 channels are configurable from n implanted electrodes. Higher

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stimulation precision and more particular spatial patterns can be delivered using limited number of implants.

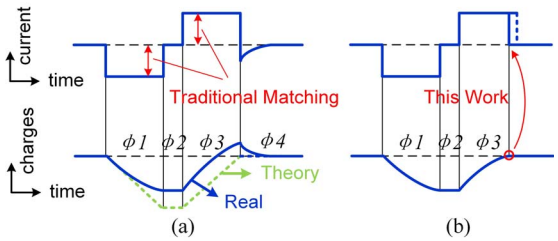


Fig. 1. Comparison of the biphasic stimulation strategies between (a) the traditional method, and (b) this work. The real charge curve derives from the ideal curve due to the charge diffusion and irreversible reaction. (Φ1: stimulation phase, Φ2: interval phase, Φ3: reversal phase, Φ4: discharge phase.)

In traditional stimulator designs, a high supply voltage is widely used to guarantee a sufficient compliance voltage, since the load impedance is unpredictable. The fixed high supply voltage leads to an unnecessary power waste. In this work, an adaptive driving voltage of the working electrode is applied. During the stimulating phase, the CE pulls current from the WE through the tissue. The driving voltage required for the WE is adjusted according to the monitoring of the CE's potential. The advantages of this proposed strategy are three-folds: i) the boosted voltage fully contributes to the stimulation process, ii) a constant low operating voltage can be used for the processing circuit, the biasing circuit, and the CE monitoring circuits, and iii) the monitoring circuits are shared with the net-zero charge detection circuits, which reduces the silicon area.

Charges carried by the ions in the physiological medium will be stored on the blocking capacitor of the CE during the stimulation phase, and the total amount of charges can be estimated by $Q_{tot} = I_{stim} \cdot t_{stim}$. Thus in the reversal phase, the CE is biased so that the current sink in the WE will first discharge these charges, when no DC power dissipation from the supply is needed.

III. Circuit Implementation

A. System Architecture

The principle of operation of this work is illustrated in Fig. 2(a), and the architecture of the system is shown in Fig. 2(b). The system integrates six driving sites, each of which can be configured as either WE or CE. Stimulation and reversal currents are generated by reversing the current path between the WE and CE. Fig. 2(c) shows the working flow. A 6-bit DAC and two comparators are integrated in the output stage of each site. One comparator is low power, which monitors the compliance voltage during the stimulating phase under the CE mode, and also monitors the blocking capacitor under the WE mode to trigger a high speed, high accuracy comparator. The high speed comparator evaluates the net charges, and terminates the reversal phase once a net-zero charge point is achieved.

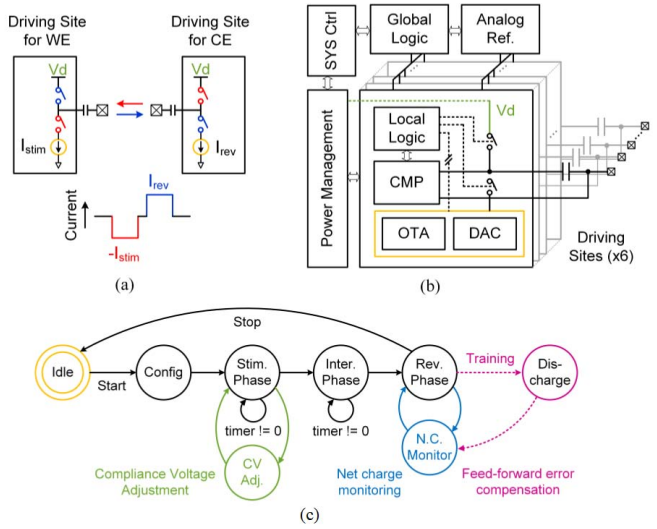


Fig. 2. (a) Basic principle of operation, (b) the block diagram of the proposed design, and (c) the state machine. A Training procedure is used during the first few stimulation pulses to calibrate the comparator for detecting the net-zero charge point.

B. Output Stage With Current Mode DAC

A transconductance amplifier (OTA) with series-series feedback is used as the current generator with high impedance. The output current can be configured by the regulating voltage or the biasing resistor. Variable resistors implemented by voltage-controlled transistors [12], and digital-set binary weighted transistors [9] have been reported, as shown in Fig. 3. But

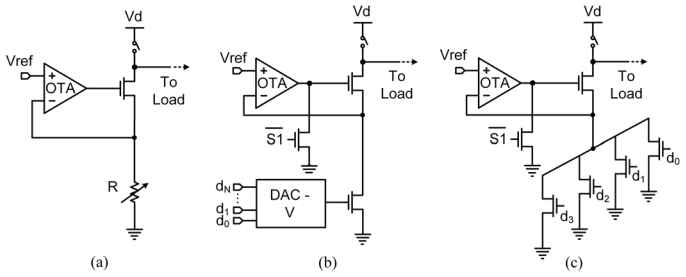


Fig. 3. (a) Basic current generator, (b) current generator with voltage-controlled transistor [12], (c) current generator with digital-set DAC [9].

the process variation leads to serious problems especially when a large number of driving sites are desired for a micro-electrode array. Typically, a calibration is required to suppress the variation, with extra cost in the die area and power. A current mode DAC with a threshold variation cancellation technique is proposed in this work to solve this problem, as shown in Fig. 4(a). Six binary weighted transistors (M1x) biased in the deep triode region are integrated with six diode-connected dummy cells (M2x). The drain current I_{dx} of M1x is set by charging M2x using a reference current I_C, as

$$I_{dx} = \mu_n C_{ox} \frac{W_1}{L_1} [(\sqrt{\frac{2I_C L_2}{\mu C_{ox} W_2}} + (V_{th2} - V_{th1}))V_{reg} - \frac{V_{reg}^2}{2}] \quad (1)$$

So I_{dx}'s variation depends on the threshold difference between M1x and M2x, which can be well cancelled. The DAC's output current can be expressed as

$$I_{DAC} = \sum_{n=0}^{5} 2^n d_n (A\sqrt{I_C} + B) \tag{2}$$

where d_n's are the input digital codes, and A, B are designable constants. The reference current I_C is shared by all driving sites. A 100-run Monte-carlo simulation shows a significant improvement in deviation and linearity, as shown in Fig. 4(b).

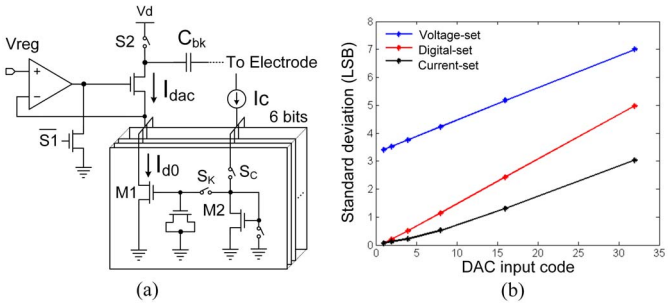


Fig. 4. (a) Output stage with the proposed current mode DAC with the threshold variation cancellation technique, and (b) a 100-run Monte-carlo simulation of the different output stage architectures with mismatch and corner variation.

C. Error Compensation Comparator

The detection of the net charge zero-crossing point is critical in this design. The propagation delay in this application includes a non-ignorable charging time for the differential input voltage to meet the resolving voltage of the comparator. The total time error is $\tau_{total} = \tau_{charge} + \tau_{pre-amp} + \tau_{latch}$, where the charging time depends on the stimulation current, the blocking capacitor's size and the offset of the comparator.

$$\tau_{charge} = \frac{(\pm\Delta V_{os} + V_{res})C_B}{I_{stim}} \tag{3}$$

A three-stage auto zeroing pre-amplifier with power gating and a dynamic latch with 4-bit calibration DAC are employed. The three-stage open-loop amplifiers provide the desired gain in a high power efficiency, and the auto zeroing design minimizes the offset voltage V_{os}. A dynamic latch is used to optimize the power-delay product.

A feed-forward error compensation mechanism, as shown in Fig. 5(a), is designed to minimize the charge error. Usually, a functional neural stimulation consists of trains of stimulation pulses in a fixed amplitude and pulse width, but varies in frequency in one trial. Thus, the delay of a comparator can be learnt in the first few stimulation cycles. In the first few stimulation cycles, an additional discharge phase is triggered after the reversal phase, and the residue charges are amplified and compared with two pre-defined thresholds to decide whether the residue charges are within the safe range. If not, the calibration DAC's value will be changed accordingly.

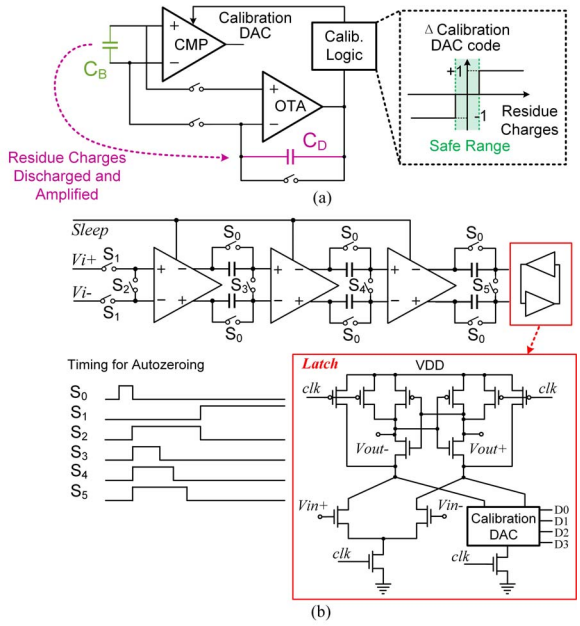
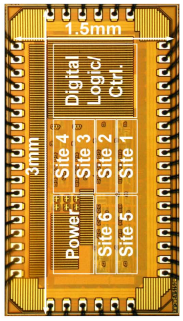


Fig. 5. (a) The feed-forward error compensation mechanism with an error detection and discharging stage using switched-capacitor circuits, and (b) the comparator consists of a 3-stages auto-zeroing pre-amplifier with power gating, and a digital latch with a calibration DAC.

IV. Experimental Result

The design has been fabricated in IBM 180nm CMOS technology. The micrograph of the chip and the chip specifications are summarized in Fig. 6. The measured INL/DNL of the DAC using conventional digital set method are 0.37/0.34 LSB, and are improved to 0.19/0.17 LSB using the proposed current-set method with threshold variation cancellation technique.



Process	180nm CMOS		
Die size	3 x 1.5 mm2		
Driving site	Num. of sites	6	
	Configurable ch.	15	
	Area per site	0.069 mm2	
	Driving voltage	+/- 3.3V	
	Compliance Range	98%	
	Stim. Current	< 2mA (depends on load)	
	Stim. Frequency	1Hz-500Hz	
	Charge error	<0.05%	
DAC	Resolution	6-bit	
	INL	0.19 LSB	
	DNL	0.17 LSB	
	Std deviation	<0.7%	
Comparator	Resolution	40μV	
	Calibration	Auto-zero/ 4-bit DAC	
	Speed	40MHz	
Power	Power per site	136 μW	
	Circuit supply	1V	
	Coin Battery	1.2V (regulator off-chip)	
	Efficiency	81% @1mA load	

Fig. 6. Die micrograph and the chip specifications summary.

Fig. 7(a) shows a measurement of the electrode voltages during the driving voltage adjustment. Stimulation currents are measured in a load of two 10nF capacitors and a 10kΩ resistor in series. A blocking capacitor of 100nF is applied. Fig. 7(b) shows the measured current across the load.

In-vitro tests are conducted using 75μm tungsten electrode in 0.9g/100mil Sodium Chloride. Fig. 8 shows the measured voltages using a traditional method (red) and the proposed method (blue) in the same driving sites under different configurations. Given the same mismatch in the current sources, a drifting of the electrode voltage when using the traditional digitally set DAC without discharge is shown in Fig. 8(a). The

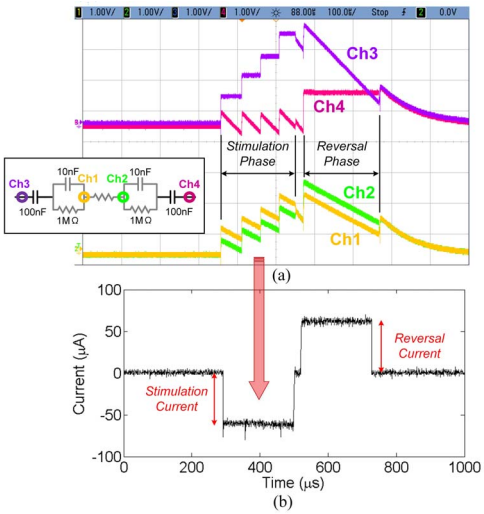


Fig. 7. (a) Measurement of a stimulus during driving voltage adjustment, and the load model with measurement points, (b) measured stimulating and reversal currents during driving voltage adaption.

measurement of the blocking capacitor's voltages in 20 trails are overlaid in Fig. 8(b), and the derived currents are plotted in Fig. 8(c). The charges over pulled in the traditional method are shown from the test in the saline solution.

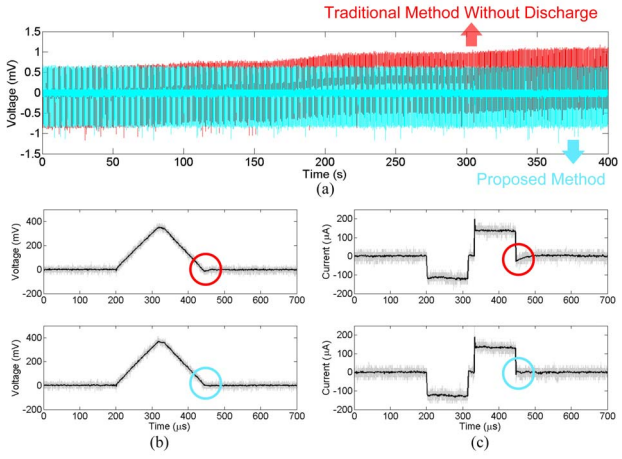


Fig. 8. Measurement of biphasic stimulation in saline solution using traditional method and the proposed method.

To demonstrate that the stimulator is capable of evoking physiological activity, an in-vivo test was performed in a sedated rat. Trains of biphasic stimulus pulses were delivered through a pair of insulated tungsten microwires, with a 50μm diameter, implanted near the intrinsic muscles that protract the mystacial vibrissae. Whisker movements, as measured by an optical micrometer, were reliably evoked as shown in Fig. 9(a). The stimulator IC was programmed by an Microcontroller with a wireless transceiver. Whisker displacements were a function of current intensity as shown in Fig. 9(b).

V. Conclusion

In this paper, a high efficiency, tissue-friendly net zero charge stimulator is proposed. The net-zero charge stimulation is achieved by controlling the timing of the reversal phase

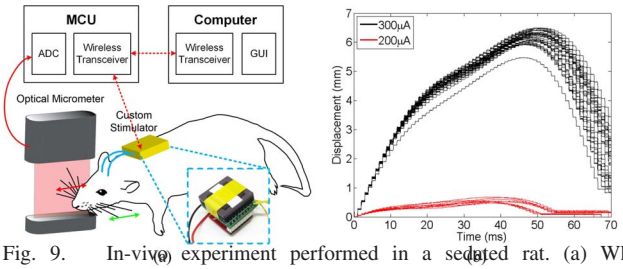


Fig. 9. In-vivo experiment performed in a sedated rat. (a) Whisker movements, as measured by an optical micrometer, were reliably evoked. (b) Whisker displacements were a function of current intensity.

based on monitoring the net charges. Arbitrary channel configuration is achieved without a pre- or on the fly calibration, which enables more dedicated stimulation position and pattern. Feed-back control of the adaptive driving voltage and stimulation charge recycling are further proposed to improve stimulation efficiency. An efficiency increase of 51% is measured in experiment. A novel current mode DAC is implemented to suppress process variation across driving site array. A digital feed-forward error compensation is used to calibrate the zero-crossing detection comparator in a continuous stimulation pulse train. In-vitro and in-vivo experiment results are shown in the paper.

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